DATA SHEET

SC2000

Universal Timeslot Interchange

Preliminary specification
File under Integrated Circuits

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Philips
Semiconductors

PHILIPS

Universal Timeslot Interchange SC2000

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FEATURES

- Multi-time slot switching capability for N x 64K channels (N = 1 to 32).
- Architecture optimized for the call processing environment: SCSA™, PEB™, or MVIP™ compatible.
- Two software selectable expansion bus formats:
  - SCbus™ /ST-BUS™
  - PEB
- Two software selectable local bus formats:
  - ST-BUS
  - PEB
- Enhanced input hysteresis threshold.
- 32 x 2048 channel switch
- Serial or parallel access to the SCbus.

- Internal support for SCbus clock fallback
- Built-in SCbus message bus interface
- Supports both Intel® and Motorola® processor interfaces
- 68-pin PLCC package
- 5v CMOS technology
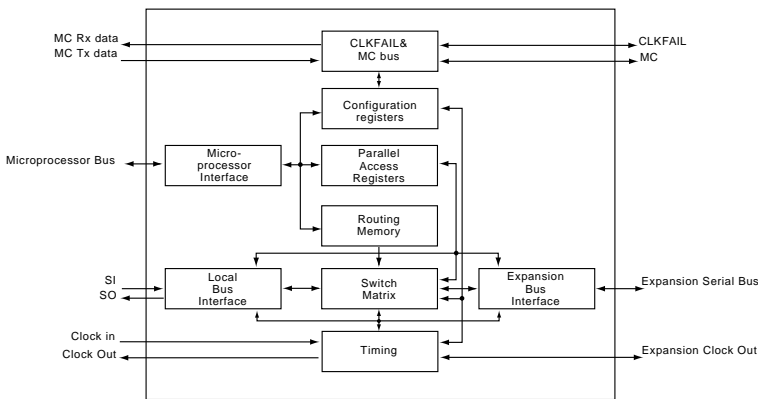
Block Diagram
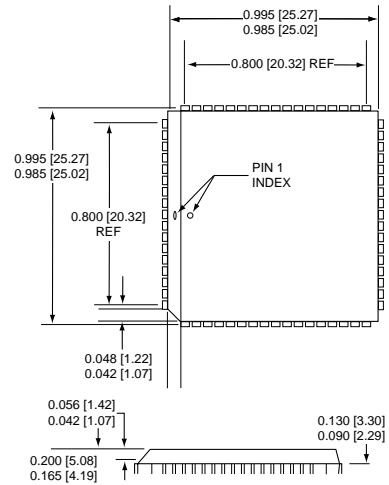
Package Mechanical Drawing

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OVERVIEW

The SC2000 is a custom VLSI circuit optimized for use in the call processing environment. The SC2000 provides a cost-effective means of implementing the interface between a high speed internal TDM bus and an external (expansion) TDM bus. Internal buffering allows the exchange of data between TDM buses of different speeds and architectures.

The SC2000 supports two external bus formats; SCbus/ST-BUS and PEB, and two internal bus formats; SCbus/ST-BUS and PEB. It is compatible with SCSA, PEB, or MVIP requirements. SCbus operation is also compatible with the Siemens PCM Highway.

The switching function and operational configurations of the SC2000 are fully software programmable. The processor bus interface is pin configured, allowing ease of use with a wide variety of industry-standard CPUs.

DESCRIPTION

The primary function of the SC2000 is to exchange digital data between the time slot on the local bus and the time slot on the expansion bus . A microprocessor interface allows the host CPU to define the time slots and serial streams between which the data is exchanged.

SCbus/ST-BUS Mode

In SCbus mode the serial streams of the external bus can be programmed to operate at 2.048 Mbps, 4.096 Mbps or 8.192 Mbps. The local bus will always operate at 2.048 Mbps.

The local-to-external bus switch connection is defined by the contents of the destination routing memory. There are 32 destination routing memory locations, one corresponding to each time slot of the local bus. The data stored in the destination routing memory selects the time slot and serial stream of the expansion bus to which the local bus input (SI) will be connected.

The external-to-local bus switch connection is defined by the contents of the source routing memory. There are 32 source routing memory locations, one corresponding to each time slot of the local bus. The data stored in the source routing memory selects the time slot and serial stream to which the local bus output (SO) will be connected.

Writing data into the routing memories is synchronized with the SCbus timing so that routing data is only changed on frame boundaries.

All serial data is buffered in holding registers. The entire contents of the holding register are transferred to the output registers on frame boundaries. This architecture introduces a constant one-frame delay through the switch. This constant delay allows bundled time slots to be switched.

PEB Mode

In PEB mode the serial streams of the external bus and the local bus may be selected to run at either 1.544 Mbps or 2.048 Mbps.

When PEB mode is selected, one of four PEB configurations may be used:

1. PEB resource mode, without switching.

2. PEB network mode, without switching.

3. PEB resource mode, with switching.

4. PEB network mode, with switching.

When switching is not selected the serial data is simply buffered between the local bus and the PEB. This maintains the data position relative to the multi-frame sync and allows robbed-bit or CAS signals to propagate transparently.

When switching is selected the serial data is transferred between the local and PEB buses via the switching matrix. The one-frame delay that occurs requires that robbed-bit or CAS signals be handled specially.

The advantages of modes with switching are:

- Timing delays between the local and PEB bus are decoupled by the switch matrix

- The local bus can access all PEB data lines (SERR, SERT, and L_SERT)

- SO can be set to high impedance on frame boundaries, allowing a bi-directional local bus to be implemented

Non-switching modes are the only configurations that support an interface to an asynchronous PEB.

CPU Data Switching

In addition to switching local bus serial data to and from the external bus, the SC2000 also allows the CPU to write data directly to the external bus. The chip provides a frame-sync generated interrupt which enables a group of time slots to be accessed from the same frame.

Internal Bus Data Switching

The Source Routing Memory Local Connect Enable selects the switching of data from any SI time slot to any SO time slot. This operation introduces a constant two-frame delay, as the data passes through the switch twice.

Loopback Mode

The SCbus Loopback Mode electrically isolates the SC2000 from the external bus but still allows access to the local bus. This mode is intended for isolating the board from the external bus while diagnostic tests are being run. A CLK_IN source is required for this mode. The recommended CLK_IN frequencies are 2.048 MHz, 4.096 MHz, 8.192 MHz, 16.384 MHz, or 32.768 MHz.

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Additional Features

The SO output may be set to high impedance on frame boundaries by setting the Source Routing Memory Switch Output Enable Bit. This allows outputs from multiple devices to be connected to a common line. The SO signal may also be configured as an open collector output.

The data sample position of both local and external buses is selectable between 50% and 75% of the bit width.

Logical and Physical Pinout Diagrams

SC2000

Pin	Signal	Signal	Pin
24	D_7	INT	35
26	D_6		
27	D_5	(CLKT) SCLKX2*	55
29	D_4	(FSYNCT) SCLK	57
30	D_3	(MSYNCT) RSRVD	58
31	D_2	(SERT) FSYNC*	59
32	D_1	(SIGT) CLKFAIL	61
33	D_0	(L_CLKT) SD_0	62
		(L_FSYNCT) SD_1	63
37	A_1	(L_MSYNCT) SD_2	65
38	A_0	(L_TSX*) SD_3	66
		(L_SERT) SD_4	67
23	CS*	(L_SIGT) SD_5	1
22	RD*(STRB*)	(CLKR) SD_6	3
20	WR*(R/W*)	(FSYNCR) SD_7	4
18	RESET	(MSYNCR) SD_8	5
17	I*(M)	(SERR) SD_9	7
		(SIGR) SD_10	8
		(R_CLKT) SD_11	9
		(R_FSYNCT) SD_12	11
		(R_MSYNCT) SD_13	12
		(R_TSX*) SD_14	13
		(R_SERT) SD_15	15
		(R_SIGT) MC	16
50	CLK_IN	SO_CLK	41
		SI_CLK	40
52	SYNC_IN	SO_FS	48
		SI_FS	47
		SO_MS	46
		SI_MS	44
39	SI	SO	43
54	TXD	RXD	53

PLCC68

Logical Pin Organization

SC2000
68-PIN PLCC
(TOP VIEW)
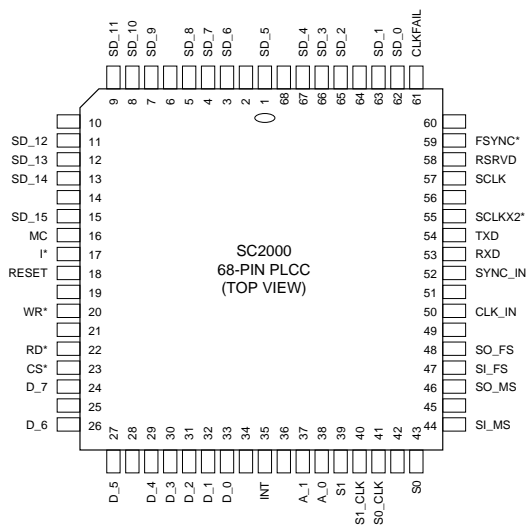
Physical Pinout

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PIN DESCRIPTION

Pin Name	Input/Output	Pin Number	Pin Description
D_0 - D_7	I/O	33, 32, 31, 30, 29, 27, 26, 24	Data bus. These bi-directional, tri-state lines are the SC2000s interface to the CPU data bus.
A_0, A_1	I	38, 37	Address bus. These inputs select the internal register used by a read or write operation. Normally connected to CPU address lines A0 and A1 in 8-bit CPU systems, or A1 and A2 in 16-bit CPU systems.
CS*	I	23	Chip Select. This active low input selects the chip for a read or write operation.
I*	I	17	Bus Interface Mode Select. This input selects Intel- and Motorola-type data bus interface configurations. 0 = Intel. 1 = Motorola.
RD* or STRB*	I I	22	I* = 0. Read This active low input enables the data bus drivers to drive the CPU data bus with the contents of the internal register selected by A_0 and A_1. I* = 1. Strobe During a read operation a low on this input enables the data bus drivers to drive the CPU data bus with the contents of the internal register selected by A_0 and A_1. During a write operation data is transferred from the CPU data bus to the register selected by A_0 and A_1 on a low to high transition of this signal.
WR* or R/W*	I I	20	I* = 0. Write During a write operation data is transferred from the CPU data bus to the register selected by A_0 and A_1 on a low to high transition of this signal. I* = 1. Read/Write This input selects between a write operation (R/W* = 0) and a read operation (R/W* =1).
RESET	I	18	Reset. This active high input forces all outputs to tri-state, and resets the SC2000 chip.
CLK_IN	I	50	Local clock input.
SYNC_IN	I	52	Local sync input.
SI	I	39	Serial input. Local serial bus data input line.
SO	O	43	Serial output. Local serial bus data output line.
TXD	I	54	Transmit data SCbus Message Bus transmit data input line.
INT	O	35	Interrupt Request. Active high interrupt request output line.
SCLKx2* or CLKT	I/O I	55	Register bit C_4 = 0. SCbus System clock x 2. Register bit C_4 = 1. PEB Transmit clock.
SCLK or FSYNCT	I/O I	57	Register bit C_4 = 0. SCbus System clock. Register bit C_4 = 1. PEB Frame sync.
RSRVD or MSYNCT	I I	58	Register bit C_4 = 0. SCbus Reserved. Register bit C_4 = 1. PEB Transmit multi-frame sync.
FSYNC* or SERT	I/O I	59	Register bit C_4 = 0. SCbus Frame sync. Register bit C_4 = 1. PEB Transmit serial data.
CLKFAIL	I/O	61	Register bit C_4 = 0. SCbus Clock fail signal.
SD_0 or L_CLKT	I/O I/O	62	Register bit C_4 = 0. SCbus Serial data stream 0. Register bit C_4 = 1. PEB Local resource transmit clock.
SD_1 or L_FSYNCT	I/O I/O	63	Register bit C_4 = 0. SCbus Serial data stream 1. Register bit C_4 = 1. PEB Local resource transmit frame sync.
SD_2 or L_MSYNCT	I/O I/O	65	Register bit C_4 = 0. SCbus Serial data stream 2. Register bit C_4 = 1. PEB Local resource multi-frame sync.
SD_3 or L_TSX*	I/O I/O	66	Register bit C_4 = 0. SCbus Serial data stream 3. Register bit C_4 = 1. PEB Local resource transmit time slot enable.

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PIN DESCRIPTION (continued)

Pin Name	Input/Output	Pin Number	Pin Description
SD_4 or L_SERT	I/O I/O	67	Register bit C_4 = 0. SCbus Serial data stream 4. Register bit C_4 = 1. PEB Local resource transmit serial data.
SD_5	I/O	1	Register bit C_4 = 0. SCbus Serial data stream 5.
SD_6 or CLKR	I/O I/O	3	Register bit C_4 = 0. SCbus Serial data stream 6. Register bit C_4 = 1. PEB Receive clock.
SD_7 or FSYNCR	I/O I/O	4	Register bit C_4 = 0. SCbus Serial data stream 7. Register bit C_4 = 1. PEB Receive frame sync.
SD_8 or MSYNCR	I/O I/O	5	Register bit C_4 = 0. SCbus Serial data stream 8. Register bit C_4 = 1. PEB Receive multi-frame sync.
SD_9 or SERR	I/O I/O	7	Register bit C_4 = 0. SCbus Serial data stream 9. Register bit C_4 = 1. PEB Receive data stream.
SD_10	I/O	8	Register bit C_4 = 0. SCbus Serial data stream 10.
SD_11	I/O	9	Register bit C_4 = 0. SCbus Serial data stream 11.
SD_12	I/O	11	Register bit C_4 = 0. SCbus Serial data stream 12.
SD_13	I/O	12	Register bit C_4 = 0. SCbus Serial data stream 13.
SD_14	I/O	13	Register bit C_4 = 0. SCbus Serial data stream 14.
SD_15	I/O	15	Register bit C_4 = 0. SCbus Serial data stream 15.
MC	I/O	16	Register bit C_4 = 0. SCbus Message Bus signal.
SO_CLK	O	41	Serial Output Clock. Clock for local serial output data.
SI_CLK	O	40	Serial Input Clock. Clock for local serial input data.
SO_FS	O	48	Serial Output Frame Sync. Frame sync for local serial output data.
SI_FS	O	47	Serial Input Frame Sync. Frame sync for local serial input data.
SO_MS	O	46	Serial Output Multi-frame Sync. Multi-frame sync for local serial output data.
SI_MS	O	44	Serial Input Multi-frame Sync. Multi-frame sync for local serial input data.
RXD	O	53	Receive Data. Message channel serial data output.
VDDO1 - VDDO5	Power	2, 10, 25, 45, 60	I/O pad V_{DD}(+5 V).
VDDI1 - VDDI3	Power	19, 34, 51	Core V_{DD}(+5 V).
VSSO1 - VSSO7	Power	6, 14, 28, 42, 56, 64, 68	I/O pad VSS (GND).
VSSI1 - VSSI3	Power	21, 36, 49	Core VSS (GND).

REGISTER DESCRIPTION

Microprocessor Interface Registers
The four 8-bit Microprocessor Interface Registers comprise the command and control port for the SC2000.

Command/Status Register
Busy (CS_0): This bit is automatically set to 1 when a command that requires synchronization with the SC2000's internal state machine has been initiated. The bit is cleared to 0 when the command has been completed. The following commands require synchronization:

• Destination Routing Memory Write
• Source Routing Memory Write
• Parallel Access Destination Write
• Parallel Access Source Read

Read (CS_1): Setting this bit to 1 initiates a read of the register pointed to by the contents of the Internal Address Register. Once the BUSY bit is read as cleared to 0 the contents of the selected register will be available in the Low Byte and High Byte Data Registers. Once the READ operation is complete the READ bit is cleared automatically.

Write (CS_2): Setting this bit to 1 initiates a write to the register pointed to by the contents of the Internal Address Register. Once the busy bit has been cleared to 0 the contents of the Low Byte and High Byte Data Registers have been transferred into the selected register. Once the WRITE operation is completed the WRITE bit is cleared automatically.

Terminate (CS_3): Setting this bit to 1 terminates any command that requires synchronization with the SC2000's internal state machine. This command is needed to complete a command when the SC2000's internal state machine has stopped running due to the failure of the system clocks. The command currently being executed is completed asynchronously and the BUSY bit is cleared to 0. To restore normal operation the TERMINATE bit must be explicitly cleared to 0. This bit can be read back for verification purposes.

Command/Status Register		
BIT	R/W	Command/Status
0	R	CS_0: Busy (S)
1	W	CS_1: Read (C)
2	W	CS_2: Write (C)
3	R/W	CS_3: Terminates (C)
4		CS_4: Reserved
5		CS_5: Reserved
6		CS_6: Reserved
7	R/W	CS_7: Reset (C)
Note:	(1) Bit 0 is the LSB of the byte.	
	(2) Initiating multiple commands in a single access is not recommended.	

CPU Interface Register Map		
A_1	A_0	Register Name
0	0	Command/Status
0	1	Internal Address
1	0	Low Byte Data
1	1	High Byte Data

Low Byte Data Register		
BIT	R/W	Function
0	R/W	D_0
1	R/W	D_1
2	R/W	D_2
3	R/W	D_3
4	R/W	D_4
5	R/W	D_5
6	R/W	D_6
7	R/W	D_7
Note:	Bit 0 is the LSB of the byte.	

High Byte Data Register		
BIT	R/W	Function
0	R/W	D_8
1	R/W	D_9
2	R/W	D_10
3	R/W	D_11
4	R/W	D_12
5	R/W	D_13
6	R/W	D_14
7	R/W	D_15
Note:	Bit 0 is the LSB of the byte.	

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Internal Register Memory Map		
Values for A_7 .. A_0 (H)	Function	R/W
00 . . 03	Configuration 1 . . Configuration 4	R/W
04	Version/Revision	R/W
05 . . 7F	Reserved . . Reserved	R/W
80 . . 9F	Destn Routing . . Destn Routing	R/W
A0 . . BF	Source Routing . . Source Routing	R/W
C0 . . DF	Destn Parallel . . Destn Parallel	R/W
E0 . . FF	Source Parallel . . Source Parallel	R/W

Reset (CS_7): Setting this bit to 1 forces the SC2000 into its reset state, and initializes all internal registers. This command reproduces the function of the RESET pin. Setting this bit to 0 returns the SC2000 to normal operation. This bit can be read back for verification purposes.

Internal Registers

The internal registers are accessed by reads and writes to the Data Registers using the address held in the Internal Address Register.

Configuration Registers
Configuration Register 1(00H)

Configuration Register 1	
BIT	Function
0	C_0: Global Output Enable
1	C_1: Expansion Bus Timing Driver Enable
2 3	C_2: Framing Mode 0 C_3:Framing Mode 1
4	C_4: Expansion Bus Interface Select
5	C_5: SCbus Loopback Mode
6 7	C_6: PEB module Type 0 C_7:PEB Module Type 1
Note:	Bit 0 is the LSB of the Low Byte Data Register.

Global Output Enable (C_0): Clearing this bit to 0 forces all outputs to the high impedance state, with the exception of the microprocessor interface data bus. Setting this bit to 1 enables all outputs. This bit is cleared on RESET.

Expansion Bus Timing Driver Enable (C_1): When SCbus Mode is selected (C_4 = 0), clearing this bit to 0 disables the expansion bus timing drivers.

When PEB Resource Mode is selected (C_6, C_4 = 01), this bit has no effect.

When PEB Network Mode is selected (C_6, C_4 = 11), clearing this bit to 0 disables the expansion bus drivers CLKR, L_CLKT, FSYNCR, L_FSYNCT, MSYNCR, and L_MSYNCT. Setting this bit to 1 enables these timing drivers.

This bit is cleared on RESET.

Framing Mode (C_3, C_2): This two-bit field selects the number of bits per frame (B/F), time slots per frame (TS/F) and frames per multi-frame (F/MF) on both the local and expansion bus.

When SCbus Mode is selected (C_4 = 0), there is no multi-frame sync signal available on the expansion bus. The (00) combination of (C_3, C_2) is invalid. In this case the internal multi-frame sync will be free running, and synchronous to FSYNC.

When PEB Mode is selected (C_4 = 1) the only valid combinations of (C_3, C_2) are (00) and (01).

These bits are cleared on RESET.

Expansion Bus			
C_3, C_2	B/F	TS/F	F/MF
00	193	24	12
01	256	32	16
10	512	64	16
11	1024	128	16

Local Bus			
C_3, C_2	B/F	TS/F	F/MF
00	193	24	12
01	256	32	16
10	256	32	16
11	256	32	16

Expansion Bus Interface Select (C_4): This bit selects the expansion bus interface operating mode. Clearing this bit to 0 selects SCbus Mode. Setting this bit to 1 selects PEB Mode.

This bit is cleared on RESET.

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SCbus Loopback Mode Select (C_5):
When SCbus Mode is selected (C_4 = 0), this bit controls the SCbus loopback. Clearing this bit to 0 disables Loopback Mode. Setting this bit to 1 enables Loopback Mode.

When PEB Mode is selected (C_4 = 1) this bit has no effect.

When loopback is enabled the expansion bus timing and data bus drivers are forced to high impedance, and the data outputs are looped back internally to the corresponding inputs. This mode is used to test the SC2000 without disrupting the operation of the SCbus.

A clock must be supplied at CLK_IN for operation in Loopback Mode.

This bit is cleared on RESET.

PEB Module Type (C_7, C_6): When PEB Mode is selected (C_4 = 1) this two-bit field selects the PEB module type.

When SCbus Mode is selected (C_4 = 0) these bits have no effect.

These bits are cleared on RESET.

PEB Module Type	
C_7, C_6	**Operating Mode**
00	Resource module without switching
01	Network module without switching
10	Resource module with switching
11	Network module with switching

Configuration Register 2 (01H)

Configuration Register 2	
Bit	**Function**
0 1 2	C_8: CLK_IN Divider 0 C_9: CLK_IN Divider 1 C_10: CLK_IN Divider 2
3	C_11: SYNC_IN Format
4 5	C_12: SYNC_IN Select 0 C_13: SYNC_IN Select 1
6	C_14: PEB Network Modul Timing Select 0
7	C_15: PEB Network Modul Timing Select 1
Note:	Bit 0 is the LSB of the Low Byte Data Register.

CLK_IN Divider (C_10, C_9, C_8):
This field selects the CLK_IN division ratio used in the generation of the system source clock.

When "CLK_IN divide by 1" and SCbus Mode are selected and the expansion bus timing drivers are enabled (C_10, C_9, C_8, C_4, C_1 = 00001), then SCLKx2* is held high and the FSYNC* period is equal to 1 SCLK period.

These bits are cleared on RESET.

CLK_IN Divider	
C_10, C_9, C_8	**CLK_IN Divided By**
000	1
001	2
010	4
011	8
100	16
101	Reserved
110	Reserved
111	Reserved

SYNC_IN Format (C_11): This bit selects the SYNC_IN format to be either PEB conventional or ST-BUS. If this bit is cleared to 0 then SYNC_IN is taken to be in the PEB conventional format. If this bit is set to 1, SYNC_IN is taken to be in the ST-BUS format.

In ST-BUS format the CLK_IN signal is inverted to produce the system clock source.

This bit is cleared on RESET.

SYNC_IN Select (C_13, C_12): This two bit field selects the function of the SYNC_IN input.

These bits are cleared on RESET.

SYNC_IN Select	
C_13, C_12	**SYNC_IN Function**
00	Ignored
01	Frame sync
10	Ignored
11	Multi-frame sync

PEB Network Module Timing Select (C_15, C_14): When PEB Network Module Mode is selected (C_6, C_4, C_1 = 111), this two bit field selects the module timing mode.

Otherwise these bits have no effect.

These bits are cleared on RESET.

PEB Network Module Timing Mode	
C_15, C_14	**Timing Mode**
00	Master
01	Master, MSYNCTfi L_MSYNCT
10	Slave, MSYNCTfi MSYNCR
11	Slave, SYNC_INfi MSYNCR

Configuration Register 3 (02H)

Configuration Register 3	
Bit	**Function**
0	C_16: Expansion Bus Data Sample Position
1	C_17: Local Bus Data Sample Position
2	C_18: SCbus Output Driver
3	C_19: SO Output Driver
4	C_20: Local Bus Framing Format
5	C_21: Message Channel TXD Select
6 7	C_22: SERT Mux 0 C_23: SERT Mux 1
Note:	Bit 0 is the LSB of the Low Byte Data Register.

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Expansion Bus Data Sample Position (C_16): When SCbus Mode is selected (C_4 = 0) this bit determines the location of the sampled point in the bit cell. When this bit is cleared to 0, sampling occurs at 50% of the bit width. When this bit is set to 1, sampling occurs at 75% of the bit width.

When PEB Mode is selected (C_4 = 1) this bit has no effect, and data is always sampled at the 50% point.

SCLKx2* must be present in order to sample at the 75% point.

This bit is cleared on RESET.

Local Bus Data Sample Position (C_17): When SCbus Mode is selected (C_4 = 0) this bit determines the location of the sample point in the bit cell. When this bit is cleared to 0 sampling occurs at 50% of the bit width. When this bit is set to 1, sampling occurs at 75% of the bit width.

When PEB Mode is selected (C_4 = 1) this bit has no effect, and data is always sampled at the 50% point.

SCLKx2* must be present in order to sample at the 75% point.

This bit is cleared on RESET.

SCbus Output Driver (C_18): When SCbus Mode is selected (C_4 = 0), this bit determines the SCbus output driver type. When this bit is cleared to 0, the output drivers are configured as tri-state type. When this bit is set to 1 the output drivers are configured as open collector type.

When PEB Mode is selected (C_4 = 1) this bit has no effect. PEB outputs are always driven open collector.

All SCbus outputs are affected by this bit with the exception of CLKFAIL and MC, which are always driven open collector.

This bit is cleared on RESET.

SO Output Driver (C_19): This bit determines the SO output driver type. When this bit is cleared to 0 the output drivers are configured as tri-state. When this bit is set to 1 the output drivers are configured as open collector.

When PEB Mode without switching is selected (C_7, C_4 = 01) then SO is always enabled.

This bit is cleared on RESET.

Local Bus Framing Format (C_20): When SCbus Mode is selected (C_4 = 0) this bit determines the local bus framing format. When this bit is cleared to 0 the local bus operates with PEB conventional framing format. When this bit is set to 1 the local bus operates with ST-BUS framing format.

When PEB Mode is selected (C_4 = 1) this bit has no effect.

With ST-BUS framing format selected, SI_CLK is replaced by C4*, SI_FS by F0*, and SI_MS by M0*. SO_CLK, SO_FS and SO_MS are unaffected by the status of this bit, and continue to output PEB conventional framing.

ST-BUS Framing Format Replacements	
PEB Conventional	ST-BUS
SI_CLK	C4*
SI_FS	F0*
SI_MS	M0*

SCLKx2* must be present, or SCLK must be at least twice the local clock (CLK_IN) frequency for ST-BUS framing format to be used.

This bit is cleared on RESET.

Message Channel TXD Select (C_21): When SCbus Mode is selected (C_4 = 0) this bit determines the configuration of the TXD input. When this bit is cleared to 0, the TXD input is configured as a transparent buffer. When this bit is set to 1 the TXD input is configured as a latched buffer.

When PEB Mode is selected (C_4 = 1), this bit has no effect. MC is not used in PEB mode.

When a transparent buffer is selected (C_21 = 0), the HDLC controller should output TXD on the rising edge of SO_CLK. When a latched buffer is selected (C_21 = 1) the HDLC controller should output TXD on the falling edge of SO_CLK.

This bit is cleared on RESET.

SERT Mux (C_23, C_22): When PEB Network Mode is selected, this two bit field selects the source of data for the local bus SO serial stream.

When SCbus Mode (C_7, C_6, C_4 = xx0) or PEB Resource Mode (C_7, C_6, C_4 = 001) are selected, these bits have no effect.

PEB Data Source Stream	
C_23, C_22	Data Source
00	L_SERT
01	(L_SERT* !L_TSX*) +(SERT* L_TSX*)

Configuration Register 4 (03H)

Configuration Register 4	
Bit	Function
0	C_24: CLKFAIL latch
1	C_25: CFSYNC latch
2	C_26: CLKFAIL latch Clear*
3	C_27: FSYNC latch Clear*
4	C_28: CLKFAIL polarity
5	C_29: INT Mask*
6	C_30: INT polarity
7	C_31: INT ouput driver
Note:	Bit 0 is the LSB of the Low Byte Data Register.

CLKFAIL Latch (C_24): When SCbus Mode is selected (C_4 = 0) this bit indicates the status of the CLKFAIL latch.

0 → CLKFAIL clear
1 → CLKFAIL set

When PEB Mode is selected (C_4 = 1), this bit is always clear.

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FSYNC Latch (C_25): When SCbus Mode (C_4 = 0) or PEB Mode with switching (C_7, C_4 = 11) are selected, these bits indicate the status of the FSYNC latch.

0 → FSYNC clear
1 → FSYNC set

When a PEB Mode without switching is selected (C_7, C_4 = 01) this bit is always clear.

CLKFAIL Latch Clear* (C_26): This bit resets the CLKFAIL latch. Clearing this bit to 0 clears the CLKFAIL latch and disables CLKFAIL interrupts. Setting this bit to 1 enables CLKFAIL interrupts.

This bit is cleared on RESET.

FSYNC Latch Clear* (C_27): This bit resets the FSYNC latch. Clearing this bit to 0 clears the FSYNC latch and disables FSYNC interrupts. Setting this bit to 1 enables FSYNC interrupts.

This bit is cleared on RESET.

CLKFAIL Polarity (C_28): This bit controls the level of the CLKFAIL signal which will set the CLKFAIL latch. When this bit is cleared to 0, the CLKFAIL latch is set when the CLKFAIL signal is "lo" (0). When this bit is set to 1 the CLKFAIL latch is set when the CLKFAIL signal is "hi" (1).

The "CLKFAIL = 0" interrupt mode is used by the new clock master to determine that clock fall back has been executed effectively. The "CLKFAIL = 1" interrupt mode is used by the standby clock board to detect clock failure.

This bit should only be changed when the CLKFAIL interrupt is disabled (C_26 = 0).

This bit is cleared on RESET.

INT Mask* (C_29): This bit controls the interrupts generated by CLKFAIL and FSYNC (INT = CLKFAIL + FSYNC). When this bit is cleared to 0 all interrupts are masked. When this bit is set to 1, interrupts are enabled.

The status of this bit does not affect the CLKFAIL Latch or FSYNC Latch bits (C_24 and C_25), and these bits can still be used to determine the status of the two latches.

This bit is cleared on RESET.

INT Output Polarity (C_30): This bit controls the active level of the INT interrupt output. When this bit is cleared to 0, then the INT output is active low. When this bit is set to 1 then the INT output is active high.

This bit is cleared on RESET.

INT Output Driver (C_31): This bit controls the configuration of the INT output driver. When this bit is cleared to 0, the INT output driver is configured as open collector. When this bit is set to 1 the INT output driver is configured as totem-pole.

Version/Revision Register (04H): The Version/Revision Register is an 8-bit read-only register used to identify the version and revision status of a particular batch of SC2000s. It is recommended that a test of this field be included in all firmware interface code to ensure compatibility.

Version/Revision Register 1	
BIT	**Function**
0	Rev 0
1	Rev 1
2	Rev 2
3	Rev 3
4	Ver 0
5	Ver 1
6	Ver 2
7	Ver 3
Note:	Bit 0 is the LSB of the Low Byte Data Register.

The initial release of the SC2000 will be Version/Revision = 00H.

Destination Routing Memory (80H - 9FH): The Destination Routing Memory maps time slots from the local SI bus onto the expansion bus. Each location in the Destination Routing Memory corresponds to a time slot on the local SI bus. The contents of each location specify a time slot on the expansion bus.

Destination Routing Memory Map	
IAR	**Destination Map**
80H	Channel 0
81H	Channel 1
82H	Channel 2
.	.
.	.
9FH	Channel 31
Note:	**IAR** = Internal Address register contents. **Channel N** is equivalent to time slot N on the local SI bus.

The contents of all Destination Routing Memory Locations are cleared on RESET.

When writing data into the Destination Routing Memory the Low Byte Data Register contains a 7-bit binary field holding a time slot number, and the High Data Byte Register contains a 4-bit binary field holding a Port (stream) number. Together these two fields uniquely identify a time slot on the expansion bus which will be the destination for data from the local SI bus.

Time Slot Select (DR_6 .. DR_0): This 7-bit field specifies a time slot number between 0 and 127. DR_6 is the MSB of this field.

Destination Routing Memory LSB	
Bit	**Function**
0 1 2 3 4 5 6	DR_0: Time slot Select 0 DR_1: Time slot Select 1 DR_2: Time slot Select 2 DR_3: Time slot Select 3 DR_4: Time slot Select 4 DR_5: Time slot Select 5 DR_6: Time slot Select 6
7	DR_7: Reserved
Note:	Bit 0 is the LSB of the Low Byte Data Register.

Port Select (DR_11 .. DR_8): When SCbus mode is selected (C_4 = 0) this 4-bit field specifies an SCbus data stream number between 0 and 15. DR_11 is the MSB of this field.

When a PEB Mode with switching is selected (C_6, C_4 = 11) this 4- bit field specifies a PEB data stream. See table for details.

Destination Routing Memory MSB	
Bit	**Function**
0 1 2 3	DR_8: Port Select 0 DR_9: Port Select 1 DR_10: Port Select 2 DR_11: Port Select 3
4	DR_12: Reserved
5	DR_13: Reserved
6	DR_14: Parallel Access Enable
7	DR_15: Switch Output Enable
Note:	Bit 0 is the LSB of the High Byte Data Register.

Destination Port Select (PEB Mode)	
DR_11..DR_8	**PEB Destination**
0H	L_SERT/L_TSX*
1H	SERR
2H	R_SERT/R_TSX*
3H	SERT
4H . . . FH	Reserved . . . Reserved

Parallel Access Enable (DR_14): When this bit is cleared to 0, the SC2000 uses the local SI bus as the source of data for the expansion bus. When this bit is set to 1 the SC2000 uses the contents of the corresponding Destination Parallel Access Register as the source of expansion bus data.

Switch Output Enable (DR_15): When this bit is cleared to 0, the SC2000 expansion bus drivers are forced to the high impedance state during the specified time slot period. When this bit is set to 1 the SC2000 expansion bus drivers drive the bus during the specified time slot period.

Source Routing Memory (A0H - BFH): The Source Routing Memory maps time slots from the expansion bus onto time slots on the local SO bus. Each location in the Source Routing Memory corresponds to a time slot on the local SO bus.

Source Routing Memory	
IAR	**Source Mapping**
A0H	Channel 0
A1H	Channel 1
A2H	Channel 2
. .	. .
BFH	Channel 31
Note:	**IAR** = Internal Address register contents. **Channel N** is equivalent to time slot N on the local S0 bus.

The contents of all Source Routing Memory Location are cleared on RESET.

When writing data into the Source Routing Memory the Low Byte Data Register contains a 7-bit binary field holding a time slot number, and the High Data Byte Register contains a 4-bit binary field holding a Port (stream) number. Together these two fields uniquely identify a time slot on the expansion bus which will be used as a source of data for a time slot on the local SO bus.

Time slot Select (SR_6 .. SR_0): This 7-bit field specifies a time slot number between 0 and 127. SR_6 is the MSB of this field.

Source Routing Memory LSB	
Bit	**Function**
0 1 2 3 4 5 6	SR_0: Time Slot Select 0 SR_1: Time Slot Select 1 SR_2: Time Slot Select 2 SR_3: Time Slot Select 3 SR_4: Time Slot Select 4 SR_5: Time Slot Select 5 SR_6: Time Slot Select 6
7	SR_7: Reserved
Note:	Bit 0 is the LSB of the Low Byte Data Register.

Port Select (SR_11 .. SR_8): When SCbus Mode is selected (C_4 = 0), this 4-bit field specifies an SCbus data stream number between 0 and 15. SR_11 is the MSB of this field.

When a PEB Mode with switching is selected (C_6, C_4 = 11) this 4-bit field specifies a PEB data stream as follows:

SR_11 is the MSB of this field.

Source Routing Memory MSB	
Bit	**Function**
0 1 2 3	SR_8: Port Select 0 SR_9: Port Select 1 SR_10: Port Select 2 SR_11: Port Select 3
4	SR_12: Reserved
5	SR_13: Reserved
6	SR_14: Local Connect Enable
7	SR_15: Switch Output Enable
Note:	Bit 0 is the LSB of the High Byte Data Register.

PEB Mode Source Data Stream	
SR_11..SR_8	**Source PEB Stream**
0H	SERT Mux
1H	SERR
2H	R_SERT
3H	SERT
4H . . FH	Reserved . . Reserved

Local Connect Enable (SR_14): This bit controls the internal connection time slots on the local bus. When this bit is cleared to 0 Local Connect is disabled. When this bit is set to 1 Local Connect is enabled and a time slot on the local SI bus will be connected internally to a time slot on the local SO bus.

When Local Connect is enabled the Source Routing Memory Time slot Select bits (SR_0 .. SR_6) select the destination time slot on the local SO bus. The contents of the Port Select field (SR_8 .. SR_11) are ignored.

Switch Output Enable (SR_15): When this bit is cleared to 0 the local SO bus drivers are forced to the high impedance state during the specified time slot period. When this bit is set to 1 the local SO bus drivers drive the bus during the specified time slot period.

Destination Parallel Access Registers (C0H .. DFH): If Parallel Access and Switch Output are enabled, the device CPU can write data to the expansion bus via these SC2000 registers. The write mapping is controlled by the Destination Routing Memory. The contents of the selected Parallel Access Register will replace the contents of the local SI bus time slot that would otherwise have been transferred to the expansion bus.

Destination Parallel Access Regs	
IAR	**SI Destination**
C0H	Channel 0
C1H	Channel 1
C2H	Channel 2
. .	. .
DFH	Channel 31
Note:	**IAR** = Internal Address Register contents. **Channel N** is equivalent to time slot N on the local SI bus.

Source Parallel Access Registers (E0H .. FFH): The Source Parallel Access Registers are continually loaded with the data being written to the corresponding local SO bus time slot, irrespective of the status of the Parallel Access Enable or Switch Output Enable bits. If Local Connect is enabled this data will originate from the local SI bus.

Source Parallel Access Regs	
IAR	**SO Destination**
E0H	Channel 0
E1H	Channel 1
E2H	Channel 2
. .	. .
FFH	Channel 31
Note:	**IAR** = Internal Address Register contents. **Channel N** is equivalent to time slot N on the local SO bus.

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ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings

Symbol	Parameter	Test Conditions	Minimum	Maximum	Unit
T_S	Storage temperature		-65	150	°C
V_I	Input voltage		-0.5	7	V
P_D	Package power dissipation			1	W
Note:	1. Voltages are with respect to ground (V_{SS}) unless otherwise stated.				

Recommended DC Operating Conditions

Symbol	Parameter	Test Conditions	Minimum	Maximum	Unit
T_A	Ambient temperature		0	70	°C
V_{DD}	Supply voltage		4.75	5.25	V
Note:	1. Voltages are with respect to ground (V_{SS}) unless otherwise stated.				

DC Electrical Characteristics

Symbol	Parameter	Test Conditions	Minimum	Maximum	Unit
I_{DD}	Supply (voltage) current			100	mA
V_{IH}	Input high voltage		2.0	V_{DD}+0.5	V
V_{IL}	Input low voltage		-0.5	1.0	V
VH_{YS}	Input hysteresis voltage		±0.4		V
I_{LI}	Input leakage current	V_I= V_{DD} or V_{SS}		±10	µA
C_I	Input capacitance			7	pF
V_{OH1}	Output high voltage (1)	I_{OH} = -24 mA	2.4		V
V_{OL1}	Output low voltage (1)	I_{OL} = 24 mA		0.4	V
V_{OH2}	Output high voltage (2)	I_{OH} = -4 mA	2.4		V
V_{OL2}	Output low voltage (2)	I_{OL} = 4 mA		0.4	V
I_{LO}	Output leakage current	V_O= V_{DD} or V_{SS}		±10	µA
C_{IO}	Output or I/O capacitance			7	pF

Notes:
1. V_{OH1}, V_{OL1} apply to Expansion Bus Interface (SCbus/PEB) signals.
2. V_{OH2}, V_{OL2} apply to all other signals.
3. Voltages are with respect to ground (V_{SS}) unless otherwise stated.
4. Input hysteresis voltage: indicates that when the input is interpreted as high (2.0 volts), it will be interpreted "high" until the input is dropped below 1.6 volts. Likewise, a low input will be interpreted as "low" until the input goes above 1.4 volts.

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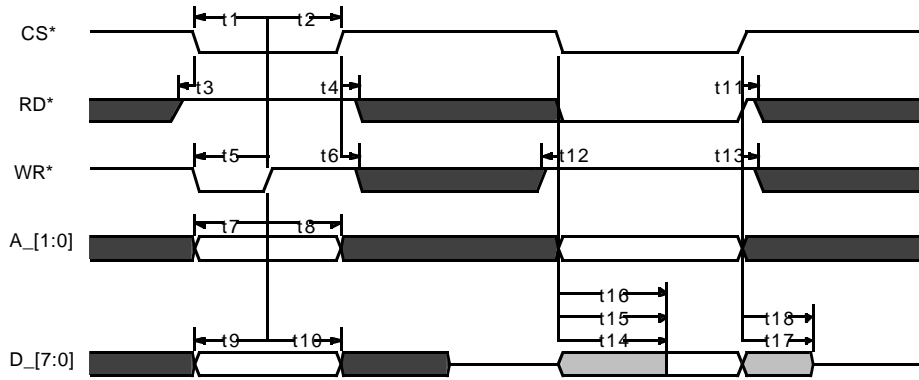**Figure 1.** Microprocessor Interface Timing — Intel Bus Mode

Table 1. Microprocessor Interface Timing — Intel Bus Mode

Symbol	Parameter	Min	Typ	Max	Unit
t1	CS* setup to WR*↑	30			ns
t2	CS* hold from WR*↑	20			ns
t3	RD* setup to CS*	10			ns
t4	RD* hold from CS*	10			ns
t5	WR* pulse width	30			ns
t6	WR* hold from CS*	10			ns
t7	A_[1:0] setup to WR*↑	30			ns
t8	A_[1:0] hold from WR*↑	20			ns
t9	D_[7:0] setup to WR*↑	30			ns
t10	D_[7:0] hold from WR*↑	20			ns
t11	RD* hold from CS*	10			ns
t12	WR* setup to CS*	10			ns
t13	WR* hold from CS*	10			ns
t14	D_[7:0] valid delay from CS*			40	ns
t15	D_[7:0] valid delay from RD*			40	ns
t16	D_[7:0] valid delay from A_[1:0]			40	ns
t17	D_[7:0] float delay from CS*			25	ns
t18	D_[7:0] float delay from RD*			25	ns
Note:	1. Timing measured with 100 pF load on D_[7:0].				

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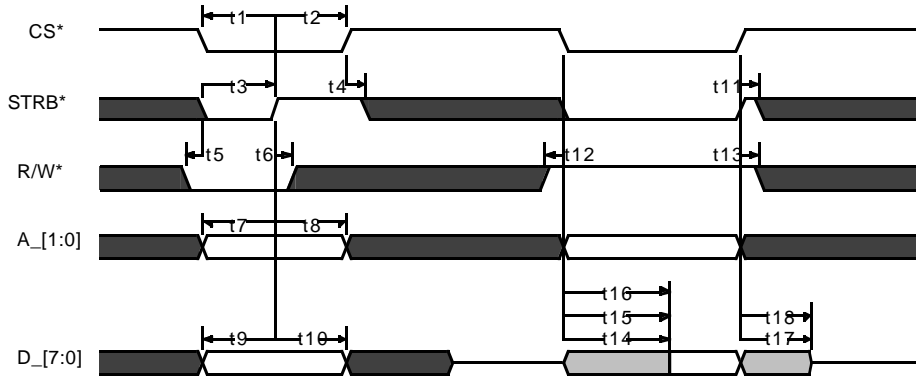**Figure 2.** Microprocessor Interface Timing — Motorola Bus Mode

Table 2. Microprocessor Interface Timing — Motorola Bus Mode

Symbol	Parameter	Min	Typ	Max	Unit
t1	CS* setup to STRB*↑	30			ns
t2	CS* hold from STRB*↑	20			ns
t3	STRB* pulse width	30			ns
t4	STRB* hold from CS*	10			ns
t5	R/W* setup to STRB*	10			ns
t6	R/W* hold from STRB*	10			ns
t7	A_[1:0] setup to STRB*↑	30			ns
t8	A_[1:0] hold from STRB*↑	20			ns
t9	D_[7:0] setup to STRB*↑	30			ns
t10	D_[7:0] hold from STRB*↑	20			ns
t11	STRB* hold from CS*	10			ns
t12	R/W*setup to STRB*	10			ns
t13	R/W*hold from STRB*	10			ns
t14	D_[7:0] valid delay from CS*			40	ns
t15	D_[7:0] valid delay from STRB*			40	ns
t16	D_[7:0] valid delay from A_[1:0]			40	ns
t17	D_[7:0] float delay from CS *			25	ns
t18	D_[7:0] float delay from STRB*			25	ns
Note:	1. Timing measured with 100 pF load on D_[7:0].				
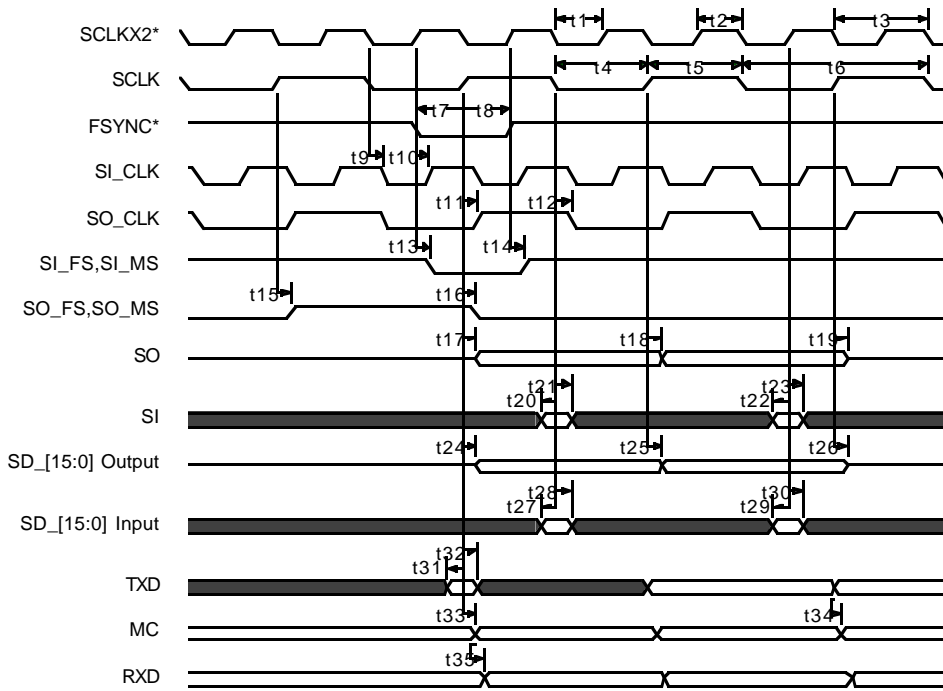
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Table 3. Local Bus Interface Timing — SCbus Mode (2.048 Mbps)

Symbol	Parameter	Min	Typ	Max	Unit
t1	SCLKx2* low time		122		ns
t2	SCLKx2* high time		122		ns
t3	SCLKx2* period		244		ns
t4	SCLK low time		244		ns
t5	SCLK high time		244		ns
t6	SCLK period		488		ns
t7	FSYNC* setup to SCLK↑	0			ns
t8	FSYNC* hold from SCLK↑	15			ns
t9	SI_CLK ↓ delay from SCLKx2* ↓			40	ns
t10	SI_CLK ↑ delay from SCLKx2* ↑			40	ns
t11	SO_CLK ↑ delay from SCLK↑			40	ns
t12	SO_CLK ↓ delay from SCLK↓			40	ns
t13	SI_FS, SI_MS ↓ delay from SCLKx2* ↑			45	ns
t14	SI_FS, SI_MS ↑ delay from SCLKx2* ↑			45	ns
t15	SO_FS, SO_MS↑ delay from SCLK↑			45	ns
t16	SO_FS, SO_MS↓ delay from SCLK↑			45	ns
t17	SO float to valid delay from SCLK↑			40	ns
t18	SO valid to valid delay from SCLK↑			40	ns
t19	SO valid to float delay from SCLK↑			25	ns
t20	SI setup to SCLK↓ (50% sample position)	0			ns
t21	SI hold from SCLK↓ (50% sample position)	25			ns
t22	SI setup to SCLKx2* ↑ (75% sample position)	0			ns
t23	SI hold from SCLKx2* ↑ (75% sample position)	25			ns
t24	SD_[15:0] float to valid delay from SCLK↑			35	ns
t25	SD_[15:0] valid to valid delay from SCLK↑			35	ns
t26	SD_[15:0] valid to float delay from SCLK↑			25	ns
t27	SD_[15:0] setup to SCLK↓ (50% sample)	0			ns
t28	SD_[15:0] hold from SCLK↓ (50% sample)	25			ns
t29	SD_[15:0] setup to SCLKx2* ↑ (75% sample)	0			ns
t30	SD_[15:0] hold from SCLKx2* ↑ (75% sample)	25			ns
t31	TXD setup to SCLK↑ (registered MC)	0			ns
t32	TXD hold from SCLK↑ (registered MC)	25			ns
t33	MC delay from SCLK↑ (registered MC)			85	ns
t34	MC delay from TXD (passed through MC			80	ns
t35	RXD delay from MC			35	ns

Notes:
1. Timing measured with 100 pF load on all Local Bus outputs, 200 pF load on all SCbus outputs.
2. MC timing measured with 200 pF, 470 Ω pullup (4.7 K Ω/10). Open collector low to high transitions include 61 ns delay from hi-Z to 2.4 V.
3. SI_CLK, SI_FS and SI_MS shown in ST-BUS framing format. When in PEB conventional framing format SI_CLK, SI_FS and SI_MS have identical timing to SO_CLK, SO_FS and SO_MS.
4. SO shown configured as tri-state driver.
5. SO_MS, SI_MS are free-running multi-frame synchronization signals that occur once every 16 frames.

Figure 4. Local Bus Interface Timing — SCbus Mode (4.096 Mbps)

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Table 4. Local Bus Interface Timing — SCbus Mode (4.096 Mbps)

| Symbol	Parameter	Min	Typ	Max	Unit
t1	SCLKx2* low time		61		ns
t2	SCLKx2* high time		61		ns
t3	SCLKx2* period		122		ns
t4	SCLK low time		122		ns
t5	SCLK high time		122		ns
t6	SCLK period		244		ns
t7	FSYNC* setup to SCLK↑	0			ns
t8	FSYNC* hold from SCLK↑	15			ns
t9	SI_CLK ↓ delay from SCLK↑			40	ns
t10	SI_CLK ↑ delay from SCLK↓			40	ns
t11	SO_CLK ↑ delay from SCLK↑			40	ns
t12	SO_CLK ↓ delay from SCLK↑			40	ns
t13	SI_FS, SI_MS ↓ delay from SCLK↓			45	ns
t14	SI_FS, SI_MS ↑ delay from SCLK↓			45	ns
t15	SO_FS, SO_MS↑ delay from SCLK↑			45	ns
t16	SO_FS, SO_MS↓ delay from SCLK↑			45	ns
t17	SO float to valid delay from SCLK↑			40	ns
t18	SO valid to valid delay from SCLK↑			40	ns
t19	SO valid to float delay from SCLK↑			25	ns
t20	SI setup to SCLK↑ (50% sample position)	0			ns
t21	SI hold from SCLK↑ (50% sample position)	25			ns
t22	SI setup to SCLK↓ (75% sample position)	0			ns
t23	SI hold from SCLK↓ (75% sample position)	25			ns
t24	SD_[15:0] float to valid delay from SCLK↑			35	ns
t25	SD_[15:0] valid to valid delay from SCLK↑			35	ns
t26	SD_[15:0] valid to float delay from SCLK↑			25	ns
t27	SD_[15:0] setup to SCLK↓ (50% sample)	0			ns
t28	SD_[15:0] hold from SCLK ↓ (50% sample)	25			ns
t29	SD_[15:0] setup to SCLKx2*↑ (75% sample)	0			ns
t30	SD_[15:0] hold from SCLKx2* ↑ (75% sample)	25			ns
t31	TXD setup to SCLK↑ (registered MC)	0			ns
t32	TXD hold from SCLK↑ (registered MC)	25			ns
t33	MC delay from SCLK↑ (registered MC)			85	ns
t34	MC delay from TXD (passed through MC)			80	ns
t35	RXD delay from MC			35	ns

Notes:
1. Timing measured with 100 pF load on all Local Bus outputs, 200 pF load on all SCbus outputs.
2. MC timing measured with 200 pF, 470 Ω pullup (4.7 K Ω/10). Open collector low to high transitions include 61 ns delay from hi-Z to 2.4 V.
3. SI_CLK, SI_FS and SI_MS shown in ST-BUS framing format. When in PEB conventional framing format SI_CLK, SI_FS and SI_MS have identical timing to SO_CLK, SO_FS and SO_MS.
4. SO shown configured as tri-state driver.
5. SO_MS, SI_MS are free-running multi-frame synchronization signals that occur once every 16 frames.

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Figure 5. Local Bus Interface Timing — SCbus Mode (8.192 Mbps)
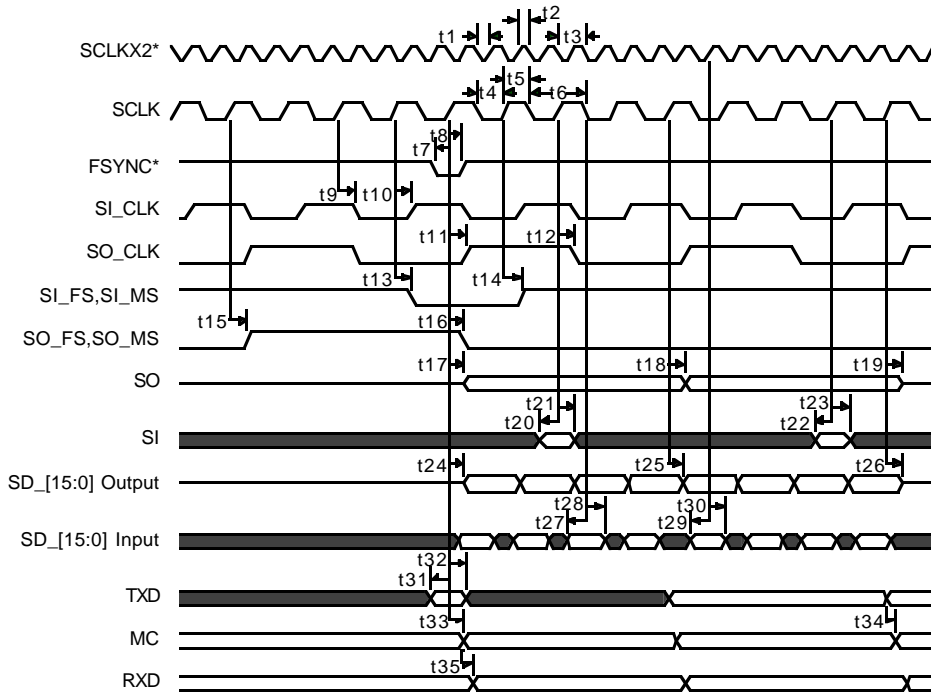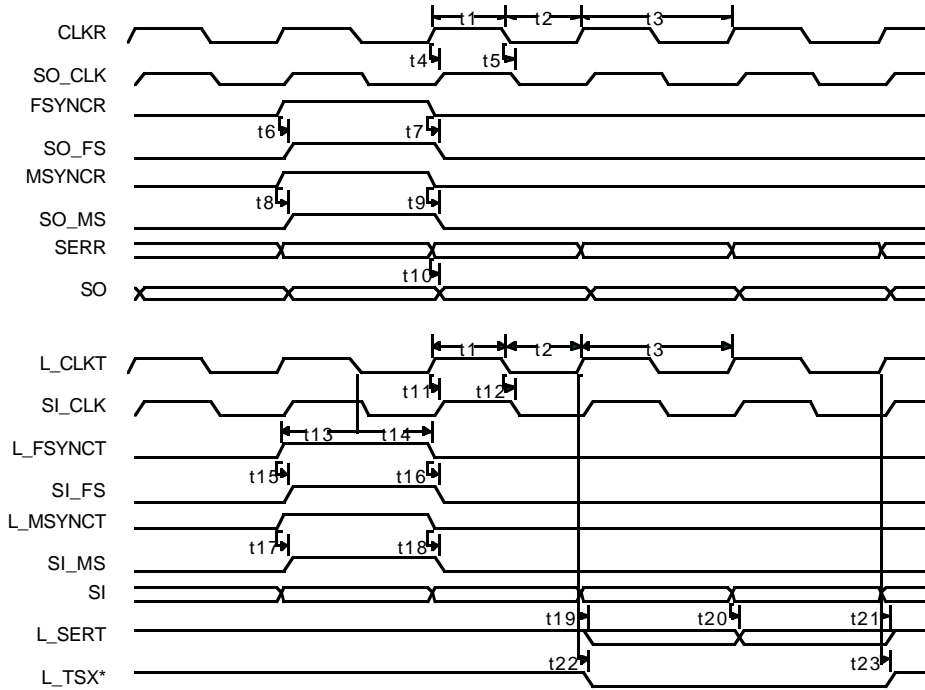
Universal Timeslot Interchange

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Table 5. Local Bus Interface Timing — SCbus Mode (8.192 Mbps)

Symbol	Parameter	Min	Typ	Max	Unit
t1	SCLKx2* low time		30.5		ns
t2	SCLKx2* high time		30.5		ns
t3	SCLKx2* period		61		ns
t4	SCLK low time		61		ns
t5	SCLK high time		61		ns
t6	SCLK period		122		ns
t7	FSYNC* setup to SCLK↑	0			ns
t8	FSYNC* hold from SCLK↑	15			ns
t9	SI_CLK↓ delay from SCLK↑			40	ns
t10	SI_CLK↑ delay from SCLK↑			40	ns
t11	SO_CLK↑ delay from SCLK↑			40	ns
t12	SO_CLK↓ delay from SCLK↑			40	ns
t13	SI_FS, SI_MS↓ delay from SCLK↑			45	ns
t14	SI_FS, SI_MS↑ delay from SCLK↑			45	ns
t15	SO_FS, SO_MS↑ delay from SCLK↑			45	ns
t16	SO_FS, SO_MS↓ delay from SCLK↑			45	ns
t17	SO float to valid delay from SCLK↑			40	ns
t18	SO valid to valid delay from SCLK↑			40	ns
t19	SO valid to float delay from SCLK↑			25	ns
t20	SI setup to SCLK↑ (50% sample position)	0			ns
t21	SI hold from SCLK↑ (50% sample position)	25			ns
t22	SI setup to SCLK↑ (75% sample position)	0			ns
t23	SI hold from SCLK↑ (75% sample position)	25			ns
t24	SD_[15:0] float to valid delay from SCLK↑			35	ns
t25	SD_[15:0] valid to valid delay from SCLK↑			35	ns
t26	SD_[15:0] valid to float delay from SCLK↑			25	ns
t27	SD_[15:0] setup to SCLK↓ (50% sample)	0			ns
t28	SD_[15:0] hold from SCLK↓ (50% sample)	25			ns
t29	SD_[15:0] setup to SCLKx2*↑ (75% sample)	0			ns
t30	SD_[15:0] hold from SCLKx2*↑ (75% sample)	25			ns
t31	TXD setup to SCLK↑ (registered MC)	0			ns
t32	TXD hold from SCLK↑ (registered MC)	25			ns
t33	MC delay from SCLK↑ (registered MC)			85	ns
t34	MC delay from TXD (passed through MC)			80	ns
t35	RXD delay from MC			35	ns

Notes:
1. Timing measured with 100 pF load on all Local Bus outputs, 200 pF load on all SCbus outputs.
2. MC timing measured with 200 pF, 470 Ω pullup (4.7 K Ω/10). Open collector low to high transitions include 61 ns delay from hi-Z to 2.4 V.
3. SI_CLK, SI_FS and SI_MS shown in ST-BUS framing format. When in PEB conventional framing format SI_CLK, SI_FS and SI_MS have identical timing to SO_CLK, SO_FS and SO_MS.
4. SO shown configured as tri-state driver.
5. SO_MS, SI_MS are free-running multi-frame synchronization signals that occur once every 16 frames.

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Figure 6. Local Bus Interface Timing — PEB Resource Module Without Switching

Table 6. Local Bus Interface Timing — PEB Resource Module Without Switching

Symbol	Parameter	Min	Typ	Max	Unit
t1a	CLKR, L_CLKT high time (1.544 Mbps)		323		ns
t1b	CLKR, L_CLKT high time (2.048 Mbps)		244		ns
t2a	CLKR, L_CLKT low time (1.544 Mbps)		323		ns
t2b	CLKR, L_CLKT low time (2.048 Mbps)		244		ns
t3a	CLKR, L_CLKT period (1.544 Mbps)		647		ns
t3b	CLKR, L_CLKT period (2.048 Mbps)		488		ns
t4	SO_CLK ↑delay from CLKR↑			35	ns
t5	SO_CLK ↓delay from CLKR↓			35	ns
t6	SO_FS ↑delay from FSYNCR↑			35	ns
t7	SO_FS ↓delay from FSYNCR↓			35	ns
t8	SO_MS ↑delay from MSYNCR↑			35	ns
t9	SO_MS ↓delay from MSYNCR↓			35	ns
t10	SO delay from SERR			35	ns
t11	SI_CLK ↑delay from L_CLKT↑			35	ns
t12	SI_CLK ↓delay from L_CLKT↓			35	ns
t13	L_FSYNCT setup to L_CLKT↓	5			ns
t14	L_FSYNCT hold from L_CLKT↓	15			ns
t15	SI_FS ↑delay from L_FSYNCT↑			35	ns
t16	SI_FS ↓delay from L_FSYNCT↓			35	ns
t17	SI_MS ↑delay from L_MSYNCT↑			35	ns
t18	SI_MS ↓delay from L_MSYNCT↓			35	ns
t19	L_SERT enable delay from L_CLKT↑			70	ns
t20	L_SERT delay from SI			60	ns
t21	L_SERT disable delay from L_CLKT↑			70	ns
t22	L_TSX*↓ delay from L_CLKT↑			35	ns
t23	L_TSX*↑ delay from L_CLKT↑			70	ns
Notes:	1. Timing measured with 100 pF load on all Local Bus outputs, 200 pF 220/330 Ω termination on all PEB outputs. Open collector low to high transitions include 43 ns delay from hi-Z to 2.4 V. 2. L_TSX* occurs on time slot boundaries.				

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Figure 7. Local Bus Interface Timing — PEB Network Module Without Switching
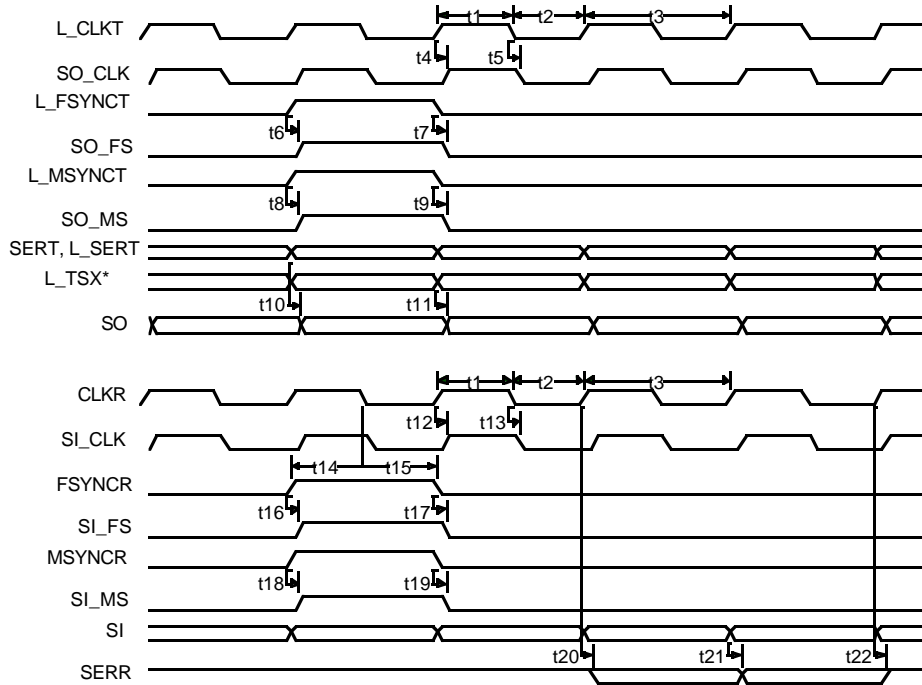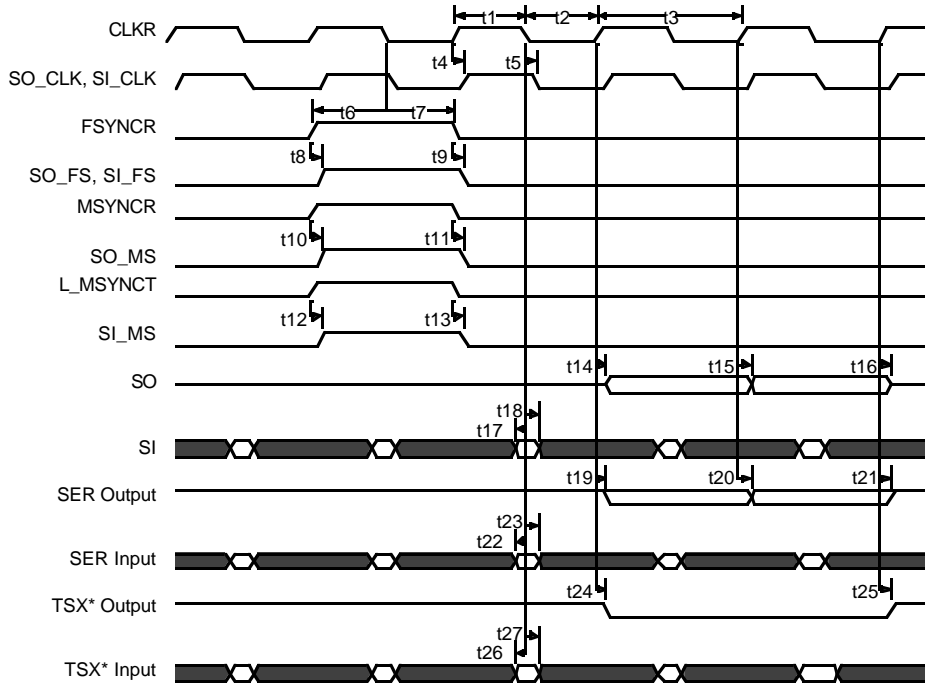
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Table 7. Local Bus Interface Timing — PEB Network Module Without Swithing

Symbol	Parameter	Min	Typ	Max	Unit
t1a	L_CLKT, CLKR high time (1.544 Mbps)		323		ns
t1b	L_CLKT, CLKR high time (2.048 Mbps)		244		ns
t2a	L_CLKT, CLKR low time (1.544 Mbps)		323		ns
t2b	L_CLKT, CLKR low time (2.048 Mbps)		244		ns
t3a	L_CLKT, CLKR period (1.544 Mbps)		647		ns
t3b	L_CLKT, CLKR period (2.048 Mbps)		488		ns
t4	SO_CLK↑ delay from L_CLKT↑			35	ns
t5	SO_CLK↓ delay from L_CLKT↓			35	ns
t6	SO_FS↑ delay from L_FSYNCT↑			35	ns
t7	SO_FS↓ delay from L_FSYNCT↓			35	ns
t8	SO_MS↑ delay from L_MSYNCT↑			35	ns
t9	SO_MS↓ delay from L_MSYNCT↓			35	ns
t10	SO delay from SERT, L_SERT			35	ns
t11	SO delay from L_TSX*			35	ns
t12	SI_CLK↑ delay from LCLKR↑			35	ns
t13	SI_CLK↓ delay from L_CLKR↓			35	ns
t14	FSYNCR setup to CLKR ↓	5			ns
t15	FSYNCR hold from CLKR ↓	15			ns
t16	SI_FS↑ delay from FSYNCR ↑			35	ns
t17	SI_FS↓ delay from FSYNCR ↓			35	ns
t18	SI_MS ↑ delay from MSYNCR↑			35	ns
t19	SI_MS ↓ delay from MSYNCR ↓			35	ns
t20	SERR enable delay from CLKR↑			70	ns
t21	SERR delay from SI			60	ns
t22	SERR disable delay from CLKR ↑			70	ns
Note:	1. Timing measured with 100 pF load on all Local Bus outputs, 200 pF 220/330 Ω termination on all PEB outputs. Open collector low to high transitions include 43 ns delay from hi-Z to 2.4 V.				

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Figure 8. Local Bus Interface Timing — PEB Resource Module With Switching
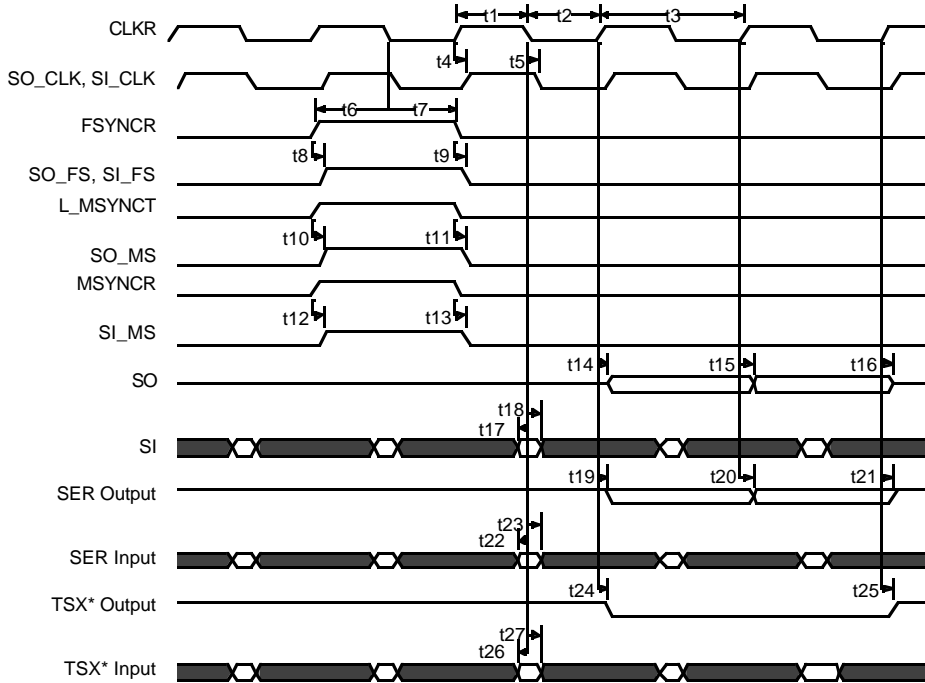
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Table 8. Local Bus Interface Timing — PEB Resource Module With Switching

Symbol	Parameter	Min	Typ	Max	Unit
t1a	CLKR high time (1.544 Mbps)		323		ns
t1b	CLKR high time (2.048 Mbps)		244		ns
t2a	CLKR low time (1.544 Mbps)		323		ns
t2b	CLKR low time (2.048 Mbps)		244		ns
t3a	CLKR period (1.544 Mbps)		647		ns
t3b	CLKR period (2.048 Mbps)		488		ns
t4	SO_CLK, SI_CLK↑ delay from CLKR ↑			35	ns
t5	SO_CLK, SI_CLK↓ delay from CLKR ↓			35	ns
t6	FSYNCR setup to CLKR ↓	5			ns
t7	FSYNCR hold from CLKR ↓	15			ns
t8	SO_FS, SI_FS↑ delay from FSYNCR ↑			35	ns
t9	SO_FS, SI_FS↓ delay from FSYNCR ↓			35	ns
t10	SO_MS↑ delay from MSYNCR↑			35	ns
t11	SO_MS↓ delay from MSYNCR ↓			35	ns
t12	SI_MS ↑ delay from L_MSYNCT ↑			35	ns
t13	SI_MS ↓ delay from L_MSYNCT↓			35	ns
t14	SO float to valid delay from CLKR↑			40	ns
t15	SO valid to valid delay from CLKR↑			40	ns
t16	SO valid to float delay from CLKR↑			25	ns
t17	SI setup to CLKR ↓	0			ns
t18	SI hold from CLKR↓	25			ns
t19	SER enable delay from CLKR↑			70	ns
t20	SER valid delay from CLKR ↑			70	ns
t21	SER disable delay from CLKR↑			70	ns
t22	SER setup to CLKR ↓	0			ns
t23	SER hold from CLKR ↓	25			ns
t24	TSX*↓ delay from CLKR↑			35	ns
t25	TSX*↑ delay from CLKR↑			70	ns
t26	TSX* setup to CLKR↓	0			ns
t27	TSX* hold from CLKR↓	25			ns
Notes:	1. Timing measured with 100 pF load on all Local Bus outputs, 200 pF 220/330 Ω termination on all PEB outputs. Open collector low to high transitions include 43 ns delay from hi-Z to 2.4 V. 2. SER = L_SERT, SERR, R_SERT, SERT. 3. TSX* = L_TSX*, R_TSX*.				

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Figure 9. Local Bus Interface Timing — PEB Network Module With Switching

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Table 9. Local Bus Interface Timing — PEB Network Module With Switching

Symbol	Parameter	Min	Typ	Max	Unit
t1a	CLKR high time (1.544 Mbps)		323		ns
t1b	CLKR high time (2.048 Mbps)		244		ns
t2a	CLKR low time (1.544 Mbps)		323		ns
t2b	CLKR low time (2.048 Mbps)		244		ns
t3a	CLKR period (1.544 Mbps)		647		ns
t3b	CLKR period (2.048 Mbps)		488		ns
t4	SO_CLK, SI_CLK↑ delay from CLKR↑			35	ns
t5	SO_CLK, SI_CLK↓ delay from CLKR↓			35	ns
t6	FSYNCR setup to CLKR↓	5			ns
t7	FSYNCR hold from CLKR↓	15			ns
t8	SO_FS, SI_FS↑ delay from FSYNCR↑			35	ns
t9	SO_FS, SI_FS↓ delay from FSYNCR↓			35	ns
t10	SO_MS↑ delay from L_MSYNCT↑			35	ns
t11	SO_MS↓ delay from L_MSYNCT↓			35	ns
t12	SI_MS↑ delay from MSYNCR↑			35	ns
t13	SI_MS↓ delay from MSYNCR↓			35	ns
t14	SO float to valid delay from CLKR↑			40	ns
t15	SO valid to valid delay from CLKR↑			40	ns
t16	SO valid to float delay from CLKR↑			25	ns
t17	SI setup to CLKR↓	0			ns
t18	SI hold from CLKR↓	25			ns
t19	SER enable delay from CLKR↑			70	ns
t20	SER valid delay from CLKR↑			70	ns
t21	SER disable delay from CLKR↑			70	ns
t22	SER setup to CLKR↓	0			ns
t23	SER hold from CLKR↓	25			ns
t24	TSX*↓ delay from CLKR↑			35	ns
t25	TSX*↑ delay from CLKR↑			70	ns
t26	TSX* setup to CLKR↓	0			ns
t27	TSX* hold from CLKR↓	25			ns
Notes:	1. Timing measured with 100 pF load on all Local Bus outputs, 200 pF 220/330 Ω termination on all PEB outputs. Open collector low to high transitions include 43 ns delay from hi-Z to 2.4 V. 2. SER = L_SERT, SERR, R_SERT, SERT. 3. TSX* = L_TSX*, R_TSX*.				

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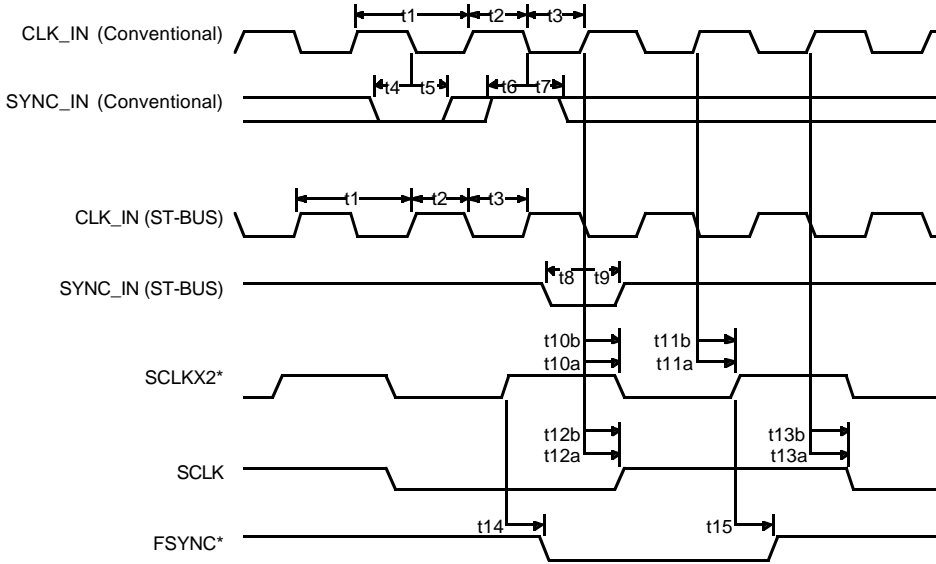**Figure 10.** CLK_IN, SYNC_IN — SCbus Mode (CLK_IN Divider ≥4)

Table 10. CLK_IN, SYNC_IN — SCbus Mode (CLK_IN Divider ≥ 4)

Symbol	Parameter	Min	Typ	Max	Unit
t1	CLK_IN period		122		ns
t2	CLK_IN high time		61		ns
t3	CLK_IN low time		61		ns
t4	SYNC_IN low setup to CLK_IN↓ (PEB conventional)	10			ns
t5	SYNC_IN low hold from CLK_IN↓ (PEB conventional)	10			ns
t6	SYNC_IN high setup to CLK_IN↓ (PEB conventional)	10			ns
t7	SYNC_IN high hold from CLK_IN↓ (PEB conventional)	10			ns
t8	SYNC_IN setup to CLK_IN↓ (ST-BUS)	10			ns
t9	SYNC_IN hold from CLK_IN↓ (ST-BUS)	10			ns
t10a	SCLKx2*↓ delay from CLK_IN↑ (PEB conventional)			25	ns
t10b	SCLKx2*↓ delay from CLK_IN↓ (ST-BUS)			25	ns
t11a	SCLKx2*↑ delay from CLK_IN↑ (PEB conventional)			25	ns
t11b	SCLKx2*↑ delay from CLK_IN↓ (ST-BUS)			25	ns
t12a	SCLK↑ delay from CLK_IN↑ (PEB conventional)			25	ns
t12b	SCLK↑ delay from CLK_IN↓ (ST-BUS)			25	ns
t13a	SCLK↓ delay from CLK_IN↑ (PEB conventional)			25	ns
t13b	SCLK↓ delay from CLK_IN↓ (ST-BUS)			25	ns
t14	FSYNC*↓ delay from SCLKx2*↑			30	ns
t15	FSYNC*↑ delay from SCLKx2*↑			30	ns
Note:	1. Timing measured with 200 pF load on all SCbus outputs.				

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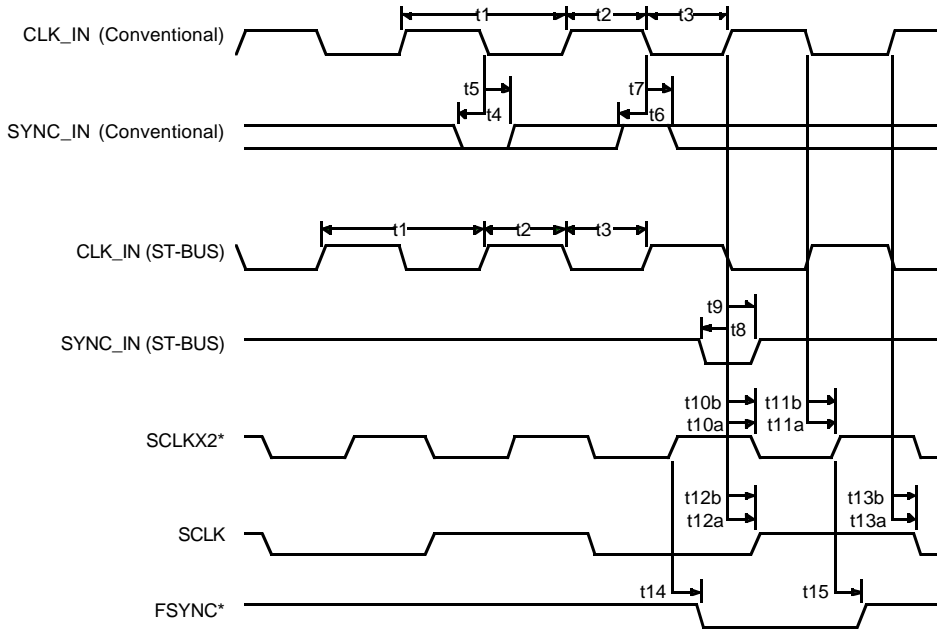
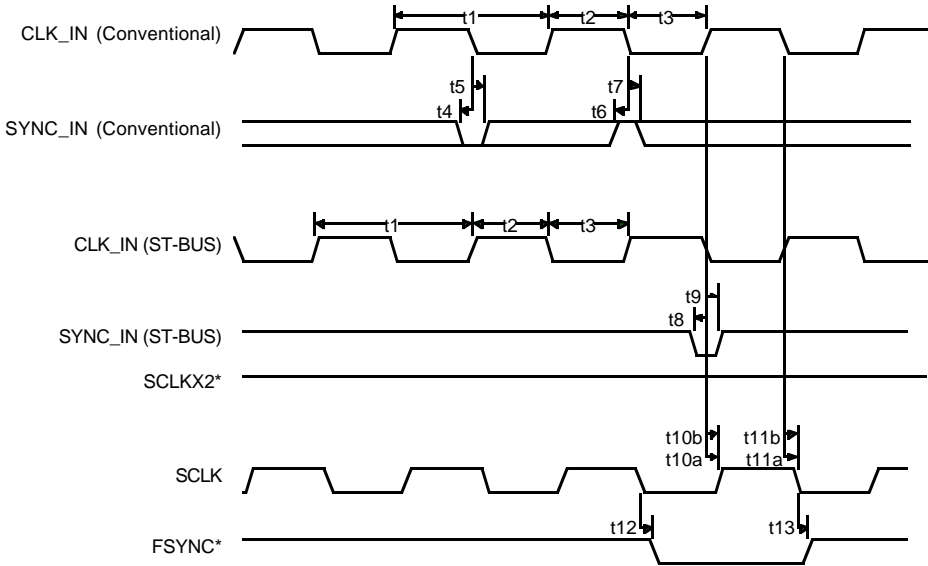**Figure 11.** CLK_IN, SYNC_IN — SCbus Mode (CLK_IN Divider = 2)

Table 11. CLK_IN, SYNC_IN — SCbus Mode (CLK_IN Divider = 2)

Symbol	Parameter	Min	Typ	Max	Unit
t1	CLK_IN period		244		ns
t2	CLK_IN high time		122		ns
t3	CLK_IN low time		122		ns
t4	SYNC_IN low setup to CLK_IN↓ (PEB conventional)	10			ns
t5	SYNC_IN low hold from CLK_IN↓ (PEB conventional)	10			ns
t6	SYNC_IN high setup to CLK_IN↓ (PEB conventional)	10			ns
t7	SYNC_IN high hold from CLK_IN↓ (PEB conventional)	10			ns
t8	SYNC_IN setup to CLK_IN↓ (ST-BUS)	10			ns
t9	SYNC_IN hold from CLK_IN↓ (ST-BUS)	10			ns
t10a	SCLKx2*↓ delay from CLK_IN↑ (PEB conventional)			25	ns
t10b	SCLKx2*↓ delay from CLK_IN↓ (ST-BUS)			25	ns
t11a	SCLKx2*↑ delay from CLK_IN↓ (PEB conventional)			25	ns
t11b	SCLKx2*↑ delay from CLK_IN↑ (ST-BUS)			25	ns
t12a	SCLK↑ delay from CLK_IN↑ (PEB conventional)			25	ns
t12b	SCLK↑ delay from CLK_IN↓ (ST-BUS)			25	ns
t13a	SCLK↓ delay from CLK_IN↑ (PEB conventional)			25	ns
t13b	SCLK↓ delay from CLK_IN↓ (ST-BUS)			25	ns
t14	FSYNC*↓ delay from SCLKx2*↑			30	ns
t15	FSYNC*↑ delay from SCLKx2*↑			30	ns
Note:	1. Timing measured with 200 pF load on all SCbus outputs.				

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**Figure 12.** CLK_IN, SYNC_IN — SCbus Mode (CLK_IN Divider = 1)

Table 12. CLK_IN, SYNC_IN — SCbus Mode (CLK_IN Divider = 1)

Symbol	Parameter	Min	Typ	Max	Unit
t1	CLK_IN period		488		ns
t2	CLK_IN high time		244		ns
t3	CLK_IN low time		244		ns
t4	SYNC_IN low setup to CLK_IN↓ (PEB conventional)	10			ns
t5	SYNC_IN low hold from CLK_IN↓ (PEB conventional)	10			ns
t6	SYNC_IN high setup to CLK_IN↓(PEB conventional)	10			ns
t7	SYNC_IN high hold from CLK_IN↓ (PEB conventional)	10			ns
t8	SYNC_IN setup to CLK_IN↓ (ST-BUS)	10			ns
t9	SYNC_IN hold from CLK_IN↓ (ST-BUS)	10			ns
t10a	SCLK↑ delay from CLK_IN↑ (PEB conventional)			25	ns
t10b	SCLK↑ delay from CLK_IN↓ (ST-BUS)			25	ns
t11a	SCLK↓ delay from CLK_IN↓ (PEB conventional)			25	ns
t11b	SCLK↓ delay from CLK_IN↑ (ST-BUS)			25	ns
t12	FSYNC*↓ delay from SCLK↓			30	ns
t13	FSYNC*↑ delay from SCLK↓			30	ns
Note:	1. Timing measured with 200 pF load on all SCbus outputs.				

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Figure 13. CLK_IN, SYNC_IN — PEB Network Master Mode (CLK_IN Divider $\geq$ 2)
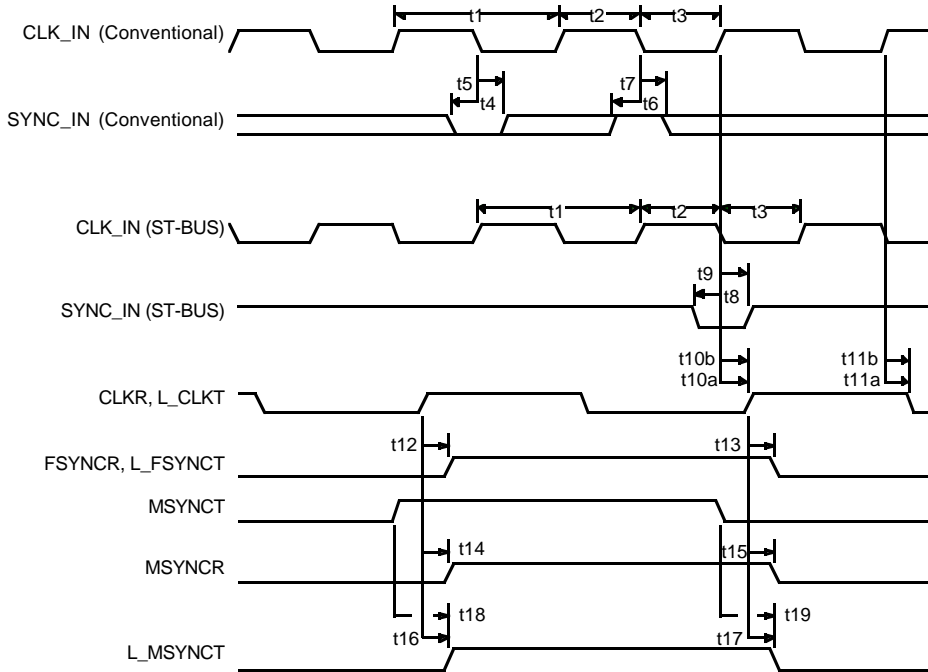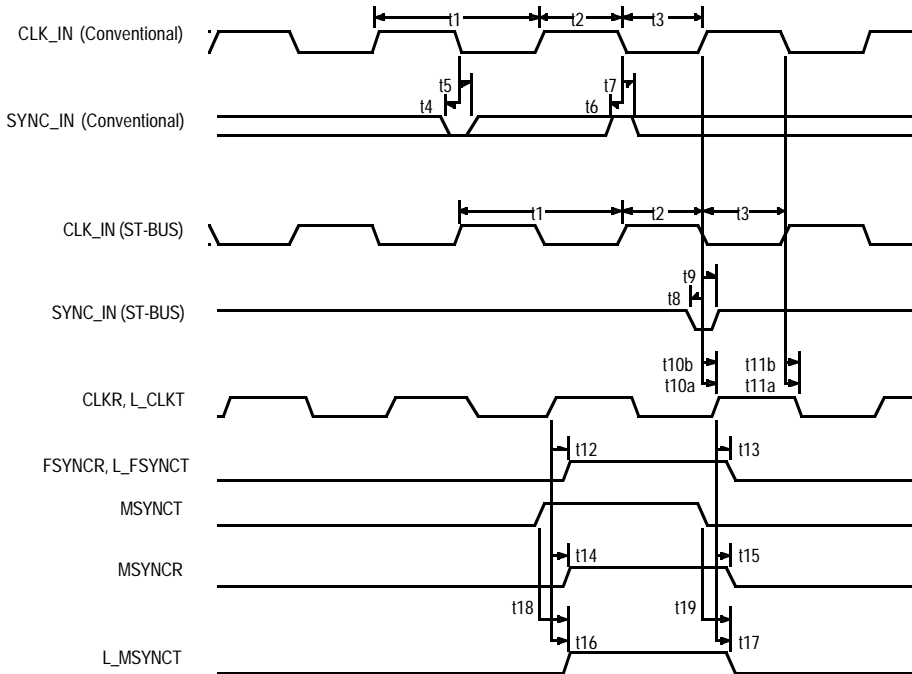
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Table 13. CLK_IN, SYNC_IN — PEB Network Master Mode (CLK_IN Divider ≥ 2)

Symbol	Parameter	Min	Typ	Max	Unit
t1	CLK_IN period		244		ns
t2	CLK_IN high time		122		ns
t3	CLK_IN low time		122		ns
t4	SYNC_IN low setup to CLK_IN↓(PEB conventional)	10			ns
t5	SYNC_IN low hold from CLK_IN↓(PEB conventional)	10			ns
t6	SYNC_IN high setup to CLK_IN↓(PEB conventional)	10			ns
t7	SYNC_IN high hold from CLK_IN↓(PEB conventional)	10			ns
t8	SYNC_IN setup to CLK_IN↓ (ST-BUS)	10			ns
t9	SYNC_IN hold from CLK_IN↓ (ST-BUS)	10			ns
t10a	CLKR, L_CLKT↑delay from CLK_IN↑(PEB conventional)			60	ns
t10b	CLKR, L_CLKT↑delay from CLK_IN↓ (ST-BUS)			60	ns
t11a	CLKR, L_CLKT↓delay from CLK_IN↑(PEB conventional)			30	ns
t11b	CLKR, L_CLKT↓delay from CLK_IN↓ (ST-BUS)			30	ns
t12	FSYNCR, L_FSYNCT↑delay from CLKR↑			70	ns
t13	FSYNCR, L_FSYNCT↓delay from CLKR↑			35	ns
t14	MSYNCR↑delay from CLKR↑			70	ns
t15	MSYNCR↓delay from CLKR↑			35	ns
t16	L_MSYNCT↑delay from CLKR↑			70	ns
t17	L_MSYNCT↓delay from CLKR↑			35	ns
t18	L_MSYNCT↑delay from MSYNCT↑			60	ns
t19	L_MSYNCT↓delay from MSYNCT↓			25	ns
Note:	1. Timing measured with 200 pF 220/330Ω termination on all PEB outputs. Open collector low to high transitions include 43 ns delay from hi-Z to 2.4 V.				

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Figure 14. CLK_IN, SYNC_IN — PEB Network Master Mode (CLK_IN Divider = 1)

Table 14. CLK_IN, SYNC_IN — PEB Network Master Mode (CLK_IN Divider = 1)

Symbol	Parameter	Min	Typ	Max	Unit
t1	CLK_IN period		488		ns
t2	CLK_IN high time		244		ns
t3	CLK_IN low time		244		ns
t4	SYNC_IN low setup to CLK_IN↓ (PEB conventional)	10			ns
t5	SYNC_IN low hold from CLK_IN↓ (PEB conventional)	10			ns
t6	SYNC_IN high setup to CLK_IN ↓ (PEB conventional)	10			ns
t7	SYNC_IN high hold from CLK_IN↓ (PEB conventional)	10			ns
t8	SYNC_IN setup to CLK_IN↓ (ST-BUS)	10			ns
t9	SYNC_IN hold from CLK_IN↓ (ST-BUS)	10			ns
t10a	CLKR, L_CLKT↑delay from CLK_IN↑(PEB conventional)			60	ns
t10b	CLKR, L_CLKT↑delay from CLK_IN↓(ST-BUS)			60	ns
t11a	CLKR, L_CLKT↓delay from CLK_IN↓(PEB conventional)			30	ns
t11b	CLKR, L_CLKT↓delay from CLK_IN↑(ST-BUS)			30	ns
t12	FSYNCR, L_FSYNCT↑delay from CLKR↑			70	ns
t13	FSYNCR, L_FSYNCT↓delay from CLKR↑			35	ns
t14	MSYNCR↑delay from CLKR↑			70	ns
t15	MSYNCR↓delay from CLKR↑			35	ns
t16	L_MSYNCT↑delay from CLKR↑			70	ns
t17	L_MSYNCT↓delay from CLKR↑			35	ns
t18	L_MSYNCT↑delay from MSYNCT↑			60	ns
t19	L_MSYNCT↓delay from MSYNCT↓			25	ns
Note:	1. Timing measured with 200 pF 220/330 Ω termination on all PEB outputs. Open collector low to high transitions include 43 ns delay from hi-Z to 2.4 V.				

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Figure 15. PEB Network Slave
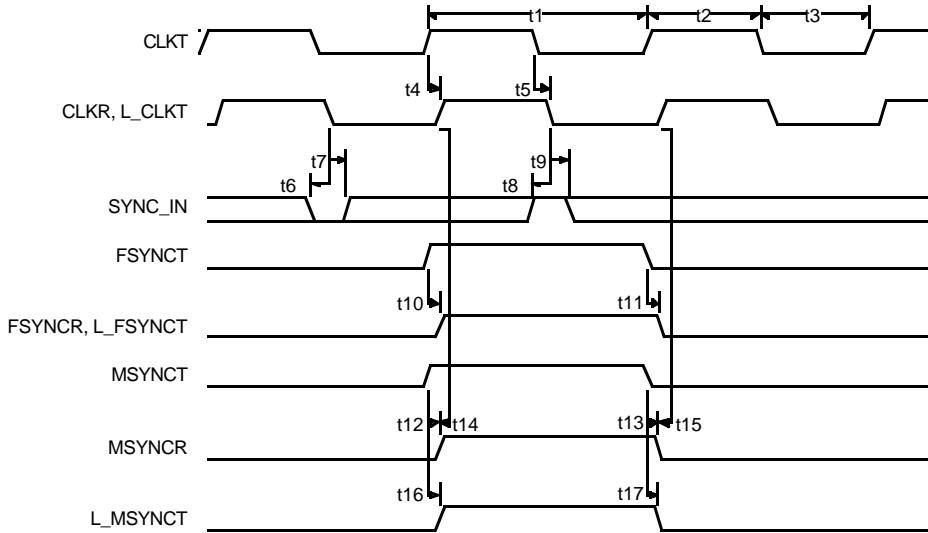
Table 15: PEB Network Slave

Symbol	Parameter	Min	Typ	Max	Unit
t1	CLKT period		488		ns
t2	CLKT high time		244		ns
t3	CLKT low time		244		ns
t4	CLKR, L_CLKT↑ delay from CLKT↑			60	ns
t5	CLKR, L_CLKT↓ delay from CLKT↓			25	ns
t6	SYNC_IN low setup to CLKR↓	0			ns
t7	SYNC_IN low hold from CLKR↓	20			ns
t8	SYNC_IN high setup to CLKR↓	0			ns
t9	SYNC_IN high hold from CLKR↓	20			ns
t10	FSYNCR, L_FSYNCT↑ delay from FSYNCT↑			60	ns
t11	FSYNCR, L_FSYNCT↓ delay from FSYNCT↓			25	ns
t12	MSYNCR↑ delay from MSYNCT↑			60	ns
t13	MSYNCR↓ delay from MSYNCT↓			25	ns
t14	MSYNCR↑ delay from CLKR↑			70	ns
t15	MSYNCR↓ delay from CLKR↑			35	ns
t16	L_MSYNCT↑ delay from MSYNCT↑			60	ns
t17	L_MSYNCT↓ delay from MSYNCT↓			25	ns
Note:	1. Timing measured with 200 pF 220/330 Ω termination on all PEB outputs. Open collector low to high transitions include 43 ns delay from hi-Z to 2.4 V.				

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SOLDERING

Introduction to soldering surface mount packages

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our *"Data Handbook IC26; Integrated Circuit Packages"* (document order number 9398 652 90011).

There is no soldering method that is ideal for all surface mount IC packages. Wave soldering can still be used for certain surface mount ICs, but it is not suitable for fine pitch SMDs. In these situations reflow soldering is recommended.

Reflow soldering

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement.

Several methods exist for reflowing; for example, convection or convection/infrared heating in a conveyor type oven. Throughput times (preheating, soldering and cooling) vary between 100 and 200 seconds depending on heating method.

Typical reflow peak temperatures range from 215 to 250 °C. The top-surface temperature of the packages should preferable be kept below 220 °C for thick/large packages, and below 235 °C for small/thin packages.

Wave soldering

Conventional single wave soldering is not recommended for surface mount devices (SMDs) or printed-circuit boards with a high component density, as solder bridging and non-wetting can present major problems.

To overcome these problems the double-wave soldering method was specifically developed.

If wave soldering is used the following conditions must be observed for optimal results:

- Use a double-wave soldering method comprising a turbulent wave with high upward pressure followed by a smooth laminar wave.

- For packages with leads on two sides and a pitch (e):
  - larger than or equal to 1.27 mm, the footprint longitudinal axis is **preferred** to be parallel to the transport direction of the printed-circuit board;
  - smaller than 1.27 mm, the footprint longitudinal axis **must** be parallel to the transport direction of the printed-circuit board.

  The footprint must incorporate solder thieves at the downstream end.

- For packages with leads on four sides, the footprint must be placed at a 45° angle to the transport direction of the printed-circuit board. The footprint must incorporate solder thieves downstream and at the side corners.

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured.

Typical dwell time is 4 seconds at 250 °C. A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

Manual soldering

Fix the component by first soldering two diagonally-opposite end leads. Use a low voltage (24 V or less) soldering iron applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C.

When using a dedicated tool, all other leads can be soldered in one operation within 2 to 5 seconds between 270 and 320 °C.

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Suitability of surface mount IC packages for wave and reflow soldering methods

PACKAGE	SOLDERING METHOD	
	WAVE	**REFLOW**[1]
BGA, LFBGA, SQFP, TFBGA	not suitable	suitable
HBCC, HLQFP, HSQFP, HSOP, HTQFP, HTSSOP, SMS	not suitable[2]	suitable
PLCC[3], SO, SOJ	suitable	suitable
LQFP, QFP, TQFP	not recommended[3][4]	suitable
SSOP, TSSOP, VSO	not recommended[5]	suitable

Notes

1. All surface mount (SMD) packages are moisture sensitive. Depending upon the moisture content, the maximum temperature (with respect to time) and body size of the package, there is a risk that internal or external package cracks may occur due to vaporization of the moisture in them (the so called popcorn effect). For details, refer to the Drypack information in the *"Data Handbook IC26; Integrated Circuit Packages; Section: Packing Methods"*.

2. These packages are not suitable for wave soldering as a solder joint between the printed-circuit board and heatsink (at bottom version) can not be achieved, and as solder may stick to the heatsink (on top version).

3. If wave soldering is considered, then the package must be placed at a 45° angle to the solder wave direction. The package footprint must incorporate solder thieves downstream and at the side corners.

4. Wave soldering is only suitable for LQFP, TQFP and QFP packages with a pitch (e) equal to or larger than 0.8 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.65 mm.

5. Wave soldering is only suitable for SSOP and TSSOP packages with a pitch (e) equal to or larger than 0.65 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.5 mm.

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DATA SHEET STATUS

DATA SHEET STATUS	PRODUCT STATUS	DEFINITIONS [1]
Objective specification	Development	This data sheet contains the design target or goal specifications for product development. Specification may change in any manner without notice.
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Note

1. Please consult the most recently issued data sheet before initiating or completing a design.

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